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# D-Band Cascode Up conversion Mixer Utilizing Double Mixing Technique for Enhanced Linearity and Output Power in 130-nm SiGe Process

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***Abstract*—This article presents a D-band cascode balanced up conversion mixer in a 130-nm SiGe process. The proposed mixer employs a double mixing technique in its cascode configuration, where the local oscillator (LO) and intermediate frequency (IF) signals are applied at the base of the common-emitter (CE) configured transistor, and the common-base (CB) configured transistor remixes the $f_{LO}$ and $f_{IF}$ signals at the collector of the CE transistor, generating additional RF signal power and thereby enhancing the overall mixing process. This up conversion mixer achieves a saturation output power of 5.9 dBm with a dc power consumption of only 69 mW. The measured output referred 1-dB compression point ($OP_{1\,dB}$) is 4.8 dBm. The measured peak conversion gain (CG) of the mixer is 9.8 dB at 139 GHz, with 3-dB bandwidth exceeding 30 GHz for different LO/IF powers. The LO-RF isolation is below −40 dB across the 120–170-GHz range. The chip size is 620 × 360 $\mu m^2$. This mixer exhibits superior performance concerning output power and linearity as well as core chip area.**

***Index Terms*—BiCMOS, cascode, D-band, double mixing, microwave monolithic integrated circuit (MMIC), mm-wave, SiGe, upconverter.**

## I. Introduction

As THE demand for high-speed communication continues to grow, researchers have been looking into wireless communication transceivers operating at millimeter-wave and subterahertz frequency ranges, where a wider bandwidth can be utilized. The frequency range of D-band (110–170 GHz) holds appeal for various compact and lightweight point-to-point uses, including backhaul connections for 5G and beyond mobile networks, communication between satellites, transmitting high-definition television (HDTV) with minimal delay wirelessly, and advanced imaging systems [1], [2], [3], [4], [5], [6].

Received 18 January 2025; revised 26 March 2025; accepted 8 April 2025. This work was supported in part by European Union through 6GTandem under Project 101096302 and in part by the Vinnova Center WiTECH, Project HiComin. *(Corresponding author: Marzie Mollaalipour.)*

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Digital Object Identifier 10.1109/TMTT.2025.3560920

In the transmitter, the up conversion mixer (or modulator) is a crucial component that receives intermediate frequency (IF) signals and then upconverts (or modulates) them to the desired RF band by using a local oscillator (LO) signal. For spectrum efficient solutions in combination with high data rates, the signal-to-noise ratio is of utmost importance; hence, the output power and linearity are the key parameters.

In addition, the mixer should have a sufficiently wide bandwidth to effectively support high data rates. Reduced power consumption and thus improved energy efficiency of the system is also a demand for future wireless systems. Furthermore, ensuring proper input impedance matching and high LO-RF isolation are essential parameters, which further complicate the design. Finally, a compact chip size is also desired.

In recent years, an increasing number of mixers operating at subterahertz frequencies have been developed in III–V, CMOS, and SiGe [7], [8], [9], [10], [11]. A recent approach involving a passive single-ended mixer with controlled LO feedthrough has demonstrated wideband operation and achieved tunable LO leakage suppression by utilizing a varactor-tuned neutralization network in the D-band [12]. However, the design suffers from relatively low conversion gain (CG) and limited linearity performance due to its passive architecture, which makes it unsuitable for applications requiring high output power. Such limitations highlight the need for innovative active mixer designs to overcome these challenges.

The double-balanced Gilbert mixer is a popular choice and employed in those active mixers. Even though the Gilbert mixer offers high CG and effective LO-RF isolation, it is typically associated with a large chip size and high dc power consumption [8], [11]. Furthermore, the stacking of transistors to handle both IF and LO signals in Gilbert-cell mixers can lead to poor linearity [13], [14]. Recent advancements have proposed improving the performance of the Gilbert mixer through modifications, such as feeding the LO signal into the transconductance stage instead of the switching quad, which doubles the input impedance, enabling lower loss matching networks and higher voltage swings for improved bandwidth and CG [15]. Another strategy involves splitting the Gilbert-cell mixer's functionality by incorporating a transformer between the transconductance and LO switching stages. This technique expands bandwidth by resonating with

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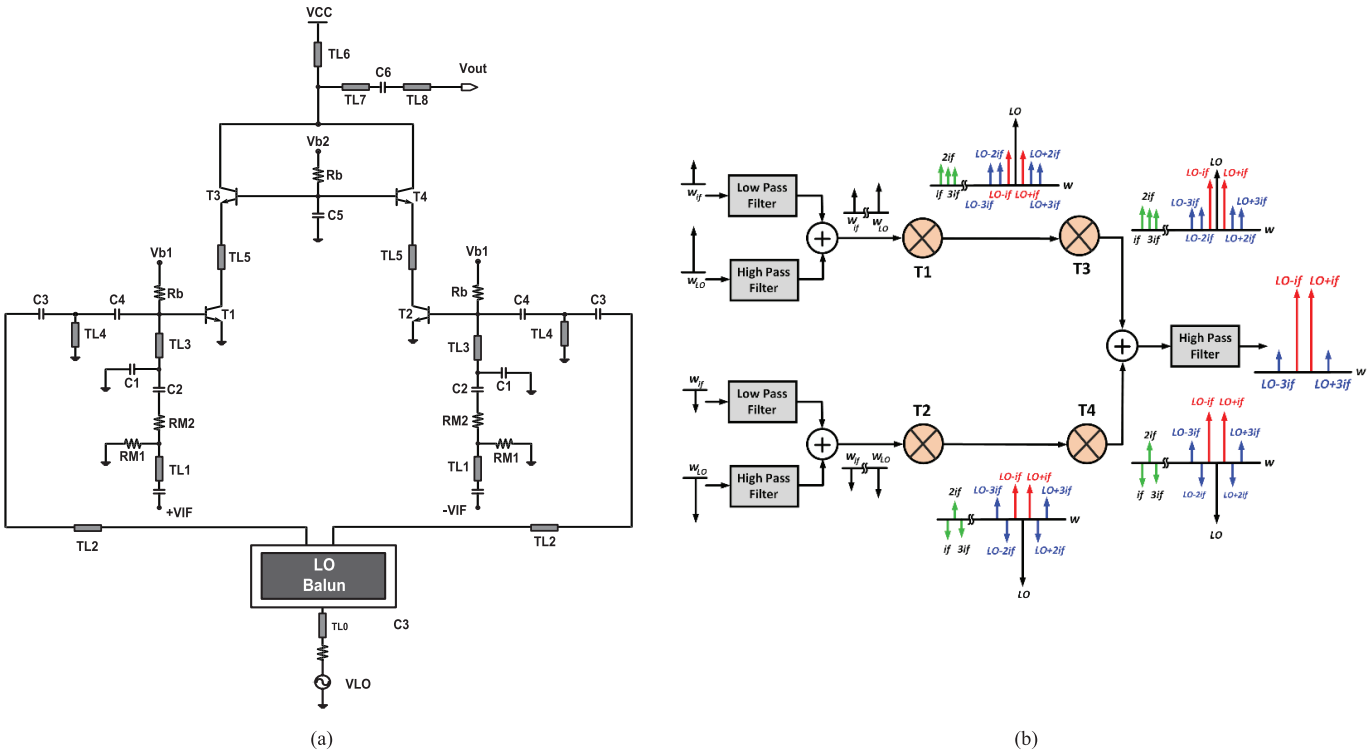


Fig. 1. (a) Circuit diagram of the proposed cascode configuration upconverter and (b) block diagram (system level) of the proposed technique.

parasitic capacitances, while a tail current source improves gain consistency and reduces power consumption [2]. Further innovation includes a current-choking mechanism using a transistor biased in the linear region to stabilize gain and reduce power consumption at high LO swings. While improving CG and mitigating signal swing issues, this approach increases design complexity and requires careful tuning to avoid nonlinear effects under PVT variations [4]. Despite these enhancements, challenges remain in achieving compact designs and higher linearity in Gilbert mixers.

Although a resistive mixer exhibits better linearity compared to a Gilbert mixer, it suffers from a significant conversion loss (>10 dB), despite not consuming dc power. On the other hand, a transconductance mixer, which consists of transistors configured in a common emitter/source arrangement, provides moderate CG and linearity [16]. In [17], a "remixer" concept was proposed for a subharmonic mixer using two cascaded stages: a transconductance subharmonic mixer followed by a common-emitter (CE) transistor. The authors suggested that the $f_{\mathrm{LO}/2} + f_{\mathrm{IF}}$ signal is remixed with the $f_{\mathrm{LO}/2}$ signal, amplifying the RF component, but this concept was not proven through simulation or experimentation. Their design also included a capacitor between the stages, which limits the lowest IF frequency and poses challenges for microwave monolithic integrated circuit (MMIC) implementation.

It is also worth mentioning that remixing does not occur in the cascoded transistors ($Q_{11}$ and $Q_{12}$ in [7, Fig. 1]), because the LO and IF signals are canceled at the emitter.

In this article, a balanced up conversion transconductance mixer in cascode configuration is proposed, employing a double mixing technique where the LO and IF signals are applied at the base of the CE configured transistor, and the common-base (CB) configured transistor further remixes these signals at the collector of the CE configured transistor, consequently improving the mixer's linearity and saturated output power.

This article is organized as follows: the proposed mixer is presented in Section II, along with the detailed circuit level design considerations. The experimental results are presented in Section III. Section IV concludes the work with a comparison to state of the art.

## II. Operation Principle of the Proposed Mixer

Fig. 1 shows the schematic of the proposed up conversion mixer with the cascode transistors.

A balanced cascode topology is proposed, and we have found that this offers several benefits for mixer applications, such as high linearity and output power, improved input/output isolation, enhanced CG, and wideband operation.

$T_1$ and $T_2$ are the input transistors of the mixer. The outputs of the common emitter configured $T_1$ and $T_2$ are connected to the common base configured $T_3$ and $T_4$ to create the cascode structure.

Both the LO and IF signals were applied to the base of $T_1$ and $T_2$ through low-pass and high-pass filters, respectively. The transconductance is modulated by the LO signal. The wanted RF signal along with LO and IF signals can be extracted from the $T_1$ and $T_2$ collectors. By feeding the produced signals into $T_3$ and $T_4$, the double mixing technique further generates fundamental RF signals through the mixing of the LO and IF signals generated in $T_1$ ($T_2$), enhancing both the linearity and output power. $T_3$ and $T_4$ not only

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provide higher RF signals at the output but also improve the input–output isolations.

To ensure a low impedance for the IF signal from the emitter of $T_3$ ($T_4$), the bases of $T_3$ and $T_4$ are connected. Because the IF signals in $T_3$ and $T_4$ are in opposite phases, the base is virtually grounded and the RF signals at the emitter of $T_3$ ($T_4$) are in the same phase. Capacitor $C_4$ has been added to provide ac grounding for the high-frequency RF signal. The design is biased for Class-B operation to achieve strong nonlinearity and low dc power consumption.

Resistive matching networks ($R_{M1}$ and $R_{M2}$) are adopted for wideband matching at the IF ports to support the high data rates. The mixer's CG and bandwidth are subject to the influence of the parasitic capacitances of the transistors in the cascode configuration. To address this, a transmission line ($TL_4$) is inserted between $T_1$ and $T_3$ ($T_2$ and $T_4$). $TL_5$ and the parasitic capacitors are utilized to form a $\pi$-network for effectively mitigating parasitic capacitance effects and improving the mixer's stability.

The overall system-level block diagram is shown in Fig. 1(b). The initial step involved applying the summation of the differential LO and IF signals to the base terminals of $T_1$ and $T_2$, facilitated by both low-pass and high-pass filters. These filters provide isolation between the LO and IF ports and impedance matching for both ports. The low-pass filter has a high frequency cutoff of 50 GHz to pass the IF signal while blocking higher frequencies, and the high-pass filter has a low frequency cutoff of 100 GHz to pass the LO signal while blocking lower frequencies. Both filters are designed as 3rd-order filters to ensure sufficient isolation and matching performance.

The fundamental RF signal in the output of $T_3$ and $T_4$ is in the same phase, while the LO and IF are in the opposite phase. Thus, the LO and IF signals are suppressed at the output port. Besides, the unwanted intermodulation components, $f_{\mathrm{LO}} \pm 2f_{\mathrm{IF}}$ and $f_{\mathrm{LO}} \pm 3f_{\mathrm{IF}}$, are also generated.

### A. Mathematical Analysis of the Cascode Configuration Employing a Double Mixing Technique

In this section, a mathematical analysis of the cascode structure is presented when it is employed in a transconductance mixer utilizing a double mixing technique.

Fig. 2 illustrates the small-signal equivalent circuit of the transconductance mixer with the cascode structure, providing a simplified representation of its behavior.

Consider an idealized transistor switching behavior, where its transconductance ($g_m$) operates, as depicted in Fig. 3(a). When a large LO signal swing is applied, the transistor's transconductance transitions into a switched waveform, as illustrated in Fig. 3(b). This waveform exhibits a duty cycle of $\alpha$, representing the fraction of time the transistor remains active within a given cycle. By expressing the $g_m$ waveform in terms of its Fourier series expansion, it can be mathematically formulated as

$$g_{mi} = g_{0i} + \sum_{n=1}^{\infty} g_{ni} \cos\left(n\omega_{\mathrm{LO}}\mathrm{t}\right), \quad i = 1, 2 \tag{1}$$

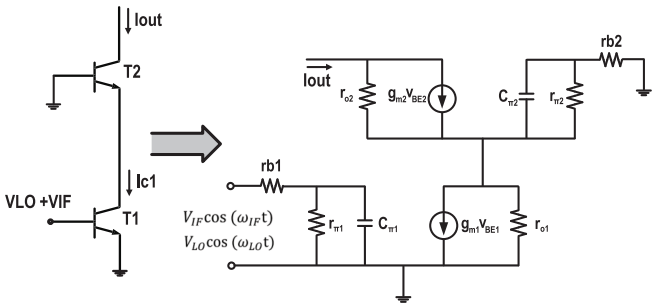


Fig. 2. Simplified small-signal equivalent circuit of a bipolar transconductance mixer with the cascode structure.

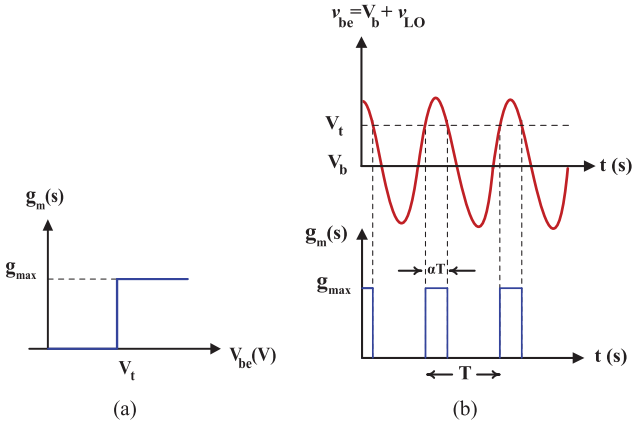


Fig. 3. (a) Transconductance of an ideal transistor. (b) Transconductance waveform [18].

where $i$ equals to 1 and 2 represents transistor $T_1$ and $T_2$, respectively.

$g_0$ denotes the average transconductance over one LO period, while $g_n$ represents the $n$th harmonic of the transconductance waveform. The Fourier coefficients are given by

$$g_0 = g_{\max} \cdot \alpha \tag{2}$$

$$g_n = \frac{2g_{\max}}{n\pi} \cdot \sin\left(n\pi\alpha\right). \tag{3}$$

These coefficients indicate the contribution of each harmonic to the overall waveform.

The collector current ($i_{c1}$) is determined by the product of the transconductance ($g_m$) and the IF voltage signal ($V_{\mathrm{IF}}$).

Substituting the expressions for $g_m$ and $v_{\mathrm{IF}}$, $i_c$ can be expanded into terms involving the RF signal and the harmonics of the LO signal. This expanded expression highlights the interaction between the LO and IF signals, leading to the generation of an RF signal at the output

$$\begin{aligned} i_{c1} &= g_{m1} \times v_{\mathrm{IF}} \\ &= g_{01} \cdot \frac{V_{\mathrm{LO}} \cos\left(\omega_{\mathrm{LO}} t\right)}{2\omega_{\mathrm{LO}} C_{\pi 1} r_{b1}} + g_{01} \cdot \frac{V_{\mathrm{IF}} \cos\left(\omega_{\mathrm{IF}} t\right)}{2\omega_{\mathrm{IF}} C_{\pi 1} r_{b1}} \\ &\quad + \frac{g_{11} \cdot V_{\mathrm{IF}}}{4\omega_{\mathrm{IF}} C_{\pi 1} r_{b1}} \cos\left(\omega_{\mathrm{LO}} - \omega_{\mathrm{IF}}\right) t \\ &\quad + \frac{g_{11} \cdot V_{\mathrm{IF}}}{4\omega_{\mathrm{IF}} C_{\pi 1} r_{b1}} \cos\left(\omega_{\mathrm{LO}} + \omega_{\mathrm{IF}}\right) t + \cdots . \end{aligned} \tag{4}$$

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By applying the same analytical process to the transconductance $g_{m2}$ of transistor $T_2$, the output current expression can be derived.

The first term in (5) represents the RF current contribution from $T_1$, which is influenced by the product $(g_{02}g_{11})$. Since $T_2$ is configured in a CB topology, its current gain remains close to unity. Consequently, the RF current generated by $T_1$ is efficiently transferred to $T_2$. This can also be verified mathematically, as the term $g_{02} \cdot r_{\pi 2}/(1 + j\omega_{\rm IF}C_{\pi 2}r_{\pi 2})$ is approximately equal to one. The second term, $(g_{12})$, accounts for the contribution from $T_2$, highlighting its role in the overall mixing process

$$i_{\rm out} = \frac{(g_{02}g_{11} + g_{12}) \cdot V_{\rm IF}r_{\pi 2}}{4\omega_{\rm IF}C_{\pi 1}r_{b1}\left(1 + j\omega_{\rm IF}C_{\pi 2}r_{\pi 2}\right)} \cos\left(\omega_{\rm LO} \pm \omega_{\rm IF}\right)t. \quad (5)$$

### *B. Cascode Transistor $T_3$ ($T_4$) Contribution to the Mixing Process*

As a thought experiment, we can compare the desired RF outputs, when the mixing function of $T_3(T_4)$ is enabled and disabled in harmonic balance simulation.

An ideal bandpass filter has been added at the output of $T_1$ ($T_2$) to filter out the low-frequency IF components only. After filtering out the IF signal, $T_3$ and $T_4$ lost the mixing function, and the output fundamental RF signal is just generated by $T_1$ and $T_2$. $T_3$ and $T_4$ function as CB configured amplifier. The system level and circuit diagram are shown in Fig. 4(a) and (b).

Figs. 5 and 6 display the harmonic balance simulation results for both the mixer configurations: with and without a filter, respectively, when LO signal has a frequency of 140 GHz and a power of 0 dBm, and IF signal has a frequency of 1 GHz and a power of −10 dBm.

The generated harmonics primarily consist of $f_{\rm IF}$ (1 GHz), $f_{\rm LO}$ (140 GHz), $f_{\rm LO} \pm f_{\rm IF}$ (139/141 GHz), $2f_{\rm IF}$ (2 GHz), $f_{\rm LO} \pm 2f_{\rm IF}$ (138/142 GHz), and $f_{\rm LO} \pm 3f_{\rm IF}$ (137/143 GHz). The red and blue colors represent the current spectrum in the output of $T_1$ ($T_2$) and $T_3$ ($T_4$), respectively.

As shown in Fig. 5, incorporating the filter to eliminate low-frequency IF components from the collector current of $T_1$ and $I_1$, the mixing function of transistor $T_3$ is disabled. Meanwhile, the ideal bandpass filter does not disturb the LO and IF signals, because the magnitudes of the inputs LO and RF signals injected into $T_3$ remain unchanged ($I_2$). The RF signal at the output of $T_3$ ($I_3$) is almost the same as $T_1$ ($I_1$) due to the near unity current gain of the CB configuration of $T_3$.

According to Fig. 6(a), by removing the filter, the IF signal at the output of $T_1$ is mixed with the LO and produces an additional RF signal. The RF current at the output of $T_3$ seems to be roughly double that of $T_1$. This doubling of the RF current is a direct result of the double mixing technique, where $T_3$ and $T_4$ further enhance the mixing process, contributing to the improved output power. Fig. 6(b) shows the current phases of $T_1$–$T_4$. As previously mentioned, the phases of the generated LO (140 GHz) and IF (1 GHz) currents in $T_1$ and $T_2$ are opposite, while the RF signals (139/141 GHz) are in the same phase. By applying the produced signals to transistors

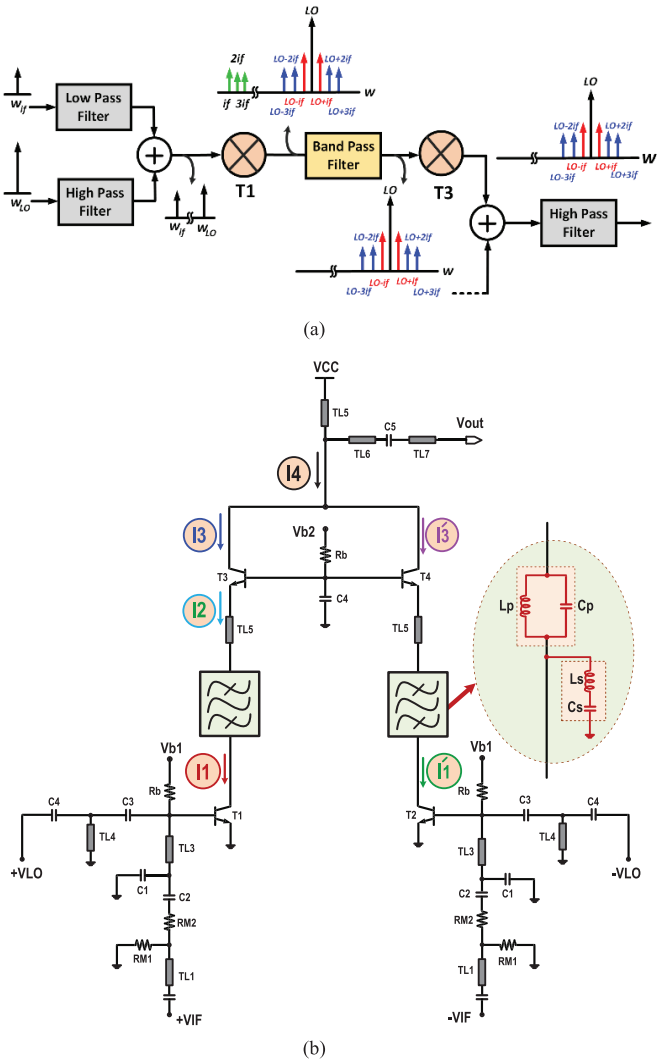


Fig. 4. (a) Block diagram (system level) and (b) circuit diagram of the cascode configuration upconverter with the deal bandpass filter.

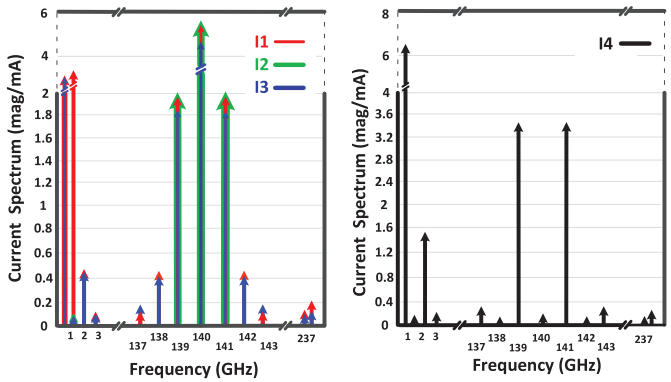


Fig. 5. Simulated spectrum of the mixer currents magnitude with the ideal bandpass filter.

$T_3$ and $T_4$, the additional RF signals generated by $T_3$ and $T_4$ are also in the same phase, as both LO and IF signals are in opposite phases.

As the outputs of $T_3$ and $T_4$ are connected, the magnitude of the $I_4$ RF signal (139/141 GHz) and $\rm IM_3$ (137/143 GHz)

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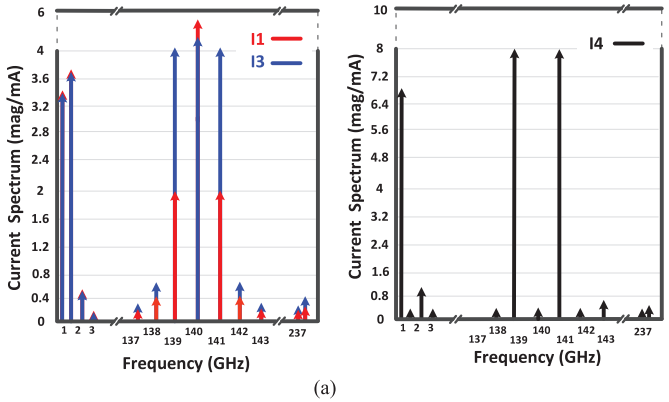
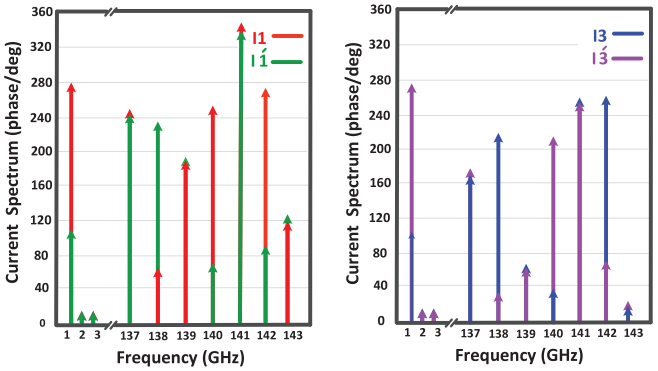



(a)




(b)

Fig. 6. Simulated spectrum of the mixer current's (a) magnitude and (b) phase without the ideal bandpass filter.

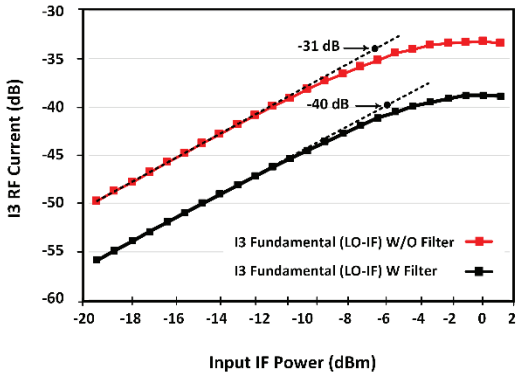



Fig. 7. $T_3$ fundamental RF currents ($I_3$) magnitude with and without filter versus input IF power.

doubles since they are in phase. Conversely, the LO (140 GHz) and $IM_2$ (138/142 GHz) signals are rejected because they are in opposite phases.

After demonstrating the improvement in output power, we discuss the contribution of the cascode transistor in enhancing the mixer's linearity for 1-dBm LO power.

To evaluate the linearity of the proposed double mixing technique, the fundamental output currents at the transistor $T_3/T_4$ (denoted as $I_3/I_4$) are presented in Fig. 7 as functions of the input IF power. These simulations are shown for both filtered and unfiltered IF currents, allowing for a

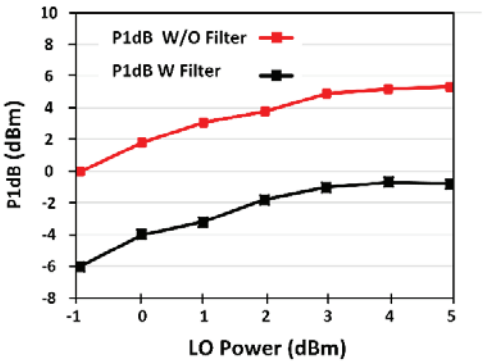



Fig. 8. Mixer's $P_{1\,\mathrm{dB}}$ with and without filter versus LO power.

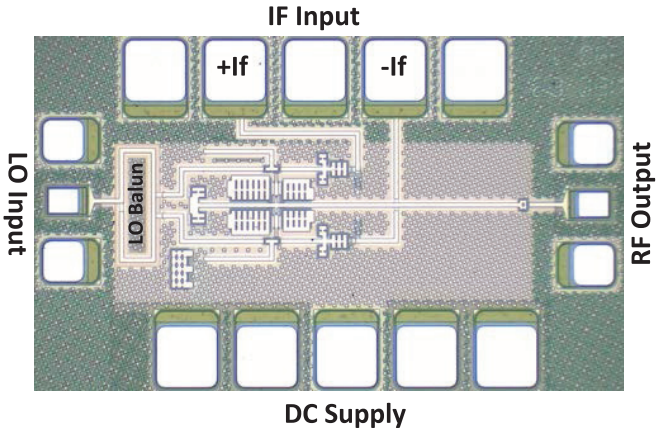



Fig. 9. Proposed mixer chip micrograph. The area is 620 × 360 $\mu$m.

comprehensive comparison. The vertical axis is displayed on a logarithmic scale to emphasize the 1-dB compression point, a key indicator of linearity. The compression characteristics of both curves demonstrate that the double mixing technique, when implemented in the cascode circuit without filtering the IF current, significantly enhances the gain. Importantly, this improvement in gain is achieved without introducing additional distortion. Thus, the double mixing technique not only improves overall gain but also preserves the mixer's high linearity performance, making it highly effective for linear high-frequency applications.

Fig. 8 illustrates the $P_{1\,\mathrm{dB}}$ as a function of LO power. The addition of the low-pass filter results in a decrease of approximately 6 dB in the output $P_{1\,\mathrm{dB}}$.

## III. Measurement Results

The up conversion mixer chip micrograph displayed in Fig. 9 is fabricated in the B11HFC 130-nm SiGe HBT technology provided by Infineon Technologies AG. The transistor features a peak $f_T$ of 250 GHz and $f_{\mathrm{Max}}$ of 390 GHz. The process provides a six-layer metal stack. The area of the chip is 620 × 360 $\mu$m$^2$, including LO balun and all pads. The chip's core is extremely compact, measuring just 410 × 180 $\mu$m$^2$, including the LO balun. Table I summarizes the design parameters of the proposed mixer.

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TABLE I
ACTIVE AND PASSIVE COMPONENTS VALUES

| TL* | TL1 | TL2 | TL3 | TL4 | TL5 | TL6 | TL7 | TL8 |
|---|---|---|---|---|---|---|---|---|
| Length(μm) | 206 | 152 | 47 | 98 | 14 | 80 | 290 | 38 |

*Width (μm): 4.9

| Cap | C1 | C2 | C3 | C4 | C5 | C6 |
|---|---|---|---|---|---|---|
| Capacitance(fF) | 120 | 320 | 26 | 26 | 3000 | 70 |

| Transistor* | T1/T2 | T3/T4 |
|---|---|---|
| Emitter Length(μm) | 18 | 15 |

*Number of fingers:2

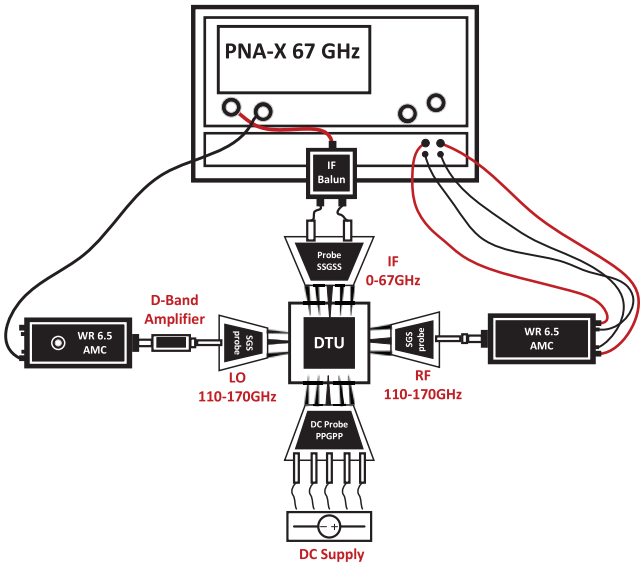


Fig. 10. Measurement setup for CG and output power.

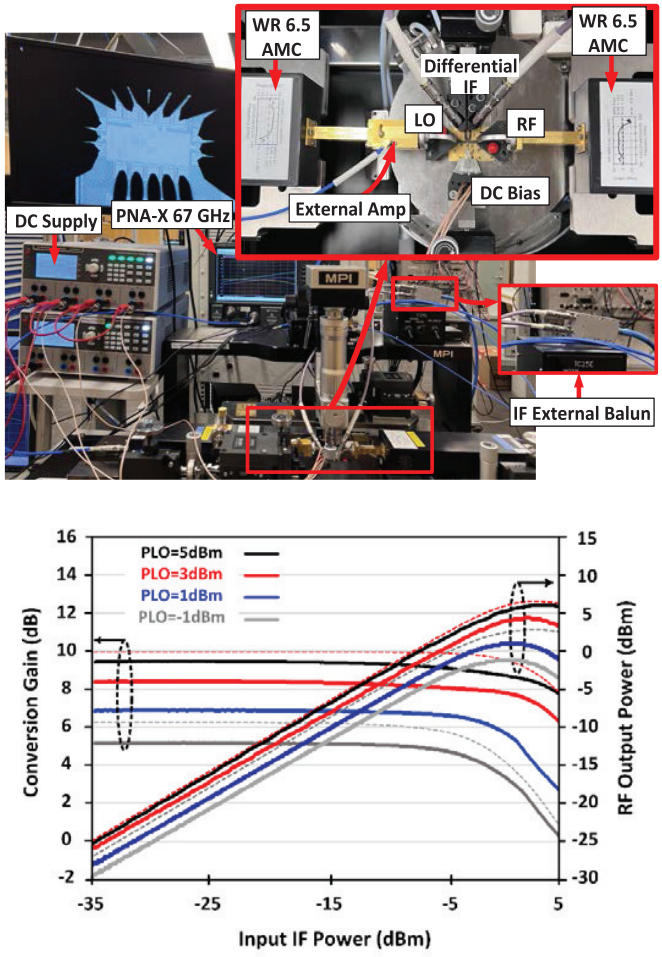


Fig. 11. Measured CG and output RF power versus input IF power with −1-, 1-, 3-, and 5-dBm LO at 140 GHz. Simulated (dashed line) CG and output power are also included.

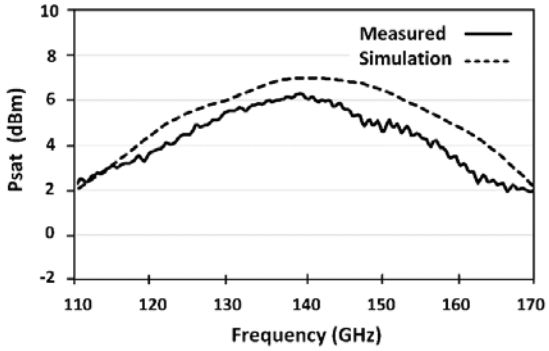


Fig. 12. Measured and simulated saturated output power of the upconverter versus LO frequency at an input frequency of 2 GHz for 4- and 2-dBm LO and IF power, respectively.

The measurement setups for CG and output power are shown in Fig. 10. Extenders were positioned at the LO (left) and RF (right) ports. The IF signal and dc supplies are delivered to the circuit via the pads at the top and bottom ports of the fabricated mixer. The IF and LO signals are generated using the PNA-X 67 GHz N5247A source. The 110–170-GHz LO signal is generated using VDI WR6.5 Amplifier multiplier chain (AMC), an active multiplier chain that boosts the frequency of an input signal. For higher LO power, a VDI WR6.5 SGX-M AMC is used, resulting in an output power of up to 8 dBm. The RF output is down-converted using another VDI WR6.5 AMC. The differential (IF) frequency signal is produced directly by the N5247A PNA-X and an external balun. Losses attributed to RF cables and probes have been individually evaluated and removed from the measurements. The LO and IF signal input powers are calibrated using the Erikson PM5 power meter, and the losses from external probes are also taken into consideration.

The mixer is probed "on wafer" using four probes. As shown in Fig. 10, three millimeter-wave probes are placed at the top, left, and right to provide connection to the on-chip IF, LO, and RF ports. For the RF and LO ports, a GSG probe featuring a 75-$\mu$m pitch and a WR6.5 waveguide interface is utilized. For the differential baseband input/output signals, a GSGSG probe with a 100-$\mu$m pitch is applied.

The measured CG for $f_{LO} - f_{IF}$ and output power versus the input power of IF signal at LO frequency of 140 GHz are presented in Fig. 11 for various LO power levels at 2-GHz IF frequency. The maximum CG reaches 9.3 dB, with a $P_{sat}$ of 5.8 dBm at 5-dBm LO power.

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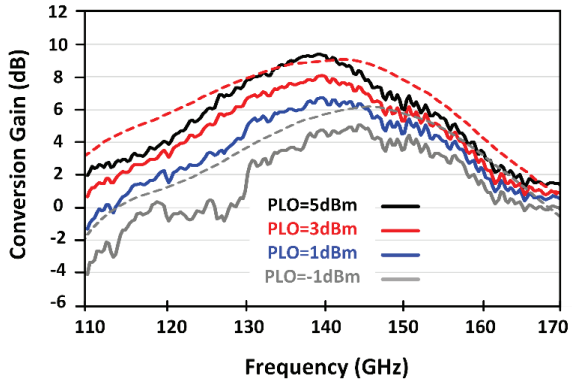


Fig. 13. Measured CG versus LO frequency at an input IF frequency of 2 GHz and −20-dBm power. Simulated (dashed line) CG with −1- and 3-dBm LO is also included.

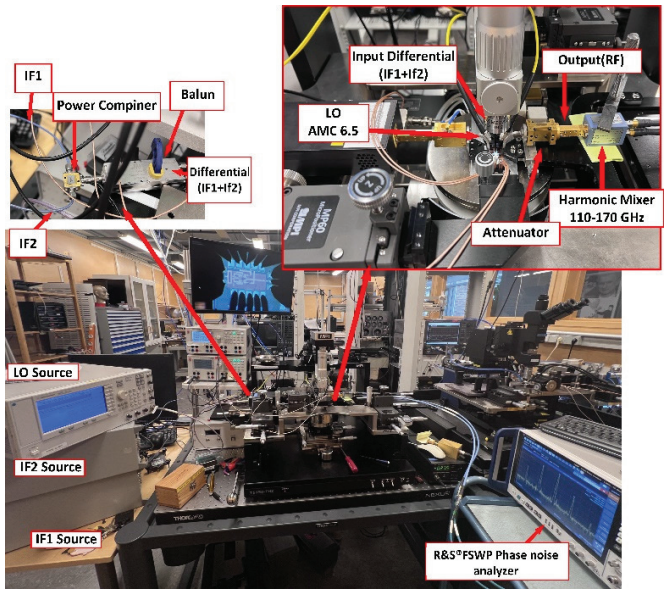


Fig. 14. $OIP_3$ measurement setup.

Simulation results are also presented, demonstrating a reasonably good agreement with the measurements. It can be seen from Fig. 12 that the mixer can deliver 6-dBm output power at 135 GHz with 3-dB bandwidth from 120 to 155 GHz at 5-dBm LO power.

Fig. 13 illustrates the simulated and measured CG versus RF frequency under various LO powers. At an LO power of 5 dBm, the measured peak CG is 9.8 dB at 137 GHz, with a 3-dB bandwidth of 25 GHz.

The $OIP_3$ measurement setup, shown in Fig. 14, and the linearity of the mixer are examined in Figs. 15 and 16. The measurement setup consists of an LO frequency source and two IF sources. It includes an R&S[1] FSWP Phase Noise Analyzer, which covers a frequency range of 1 MHz–50 GHz (extends up to 325 GHz using external mixers) along with a D-band harmonic mixer for high-frequency measurements. Fig. 15 shows the measurement results along with the

[1]Registered trademark.

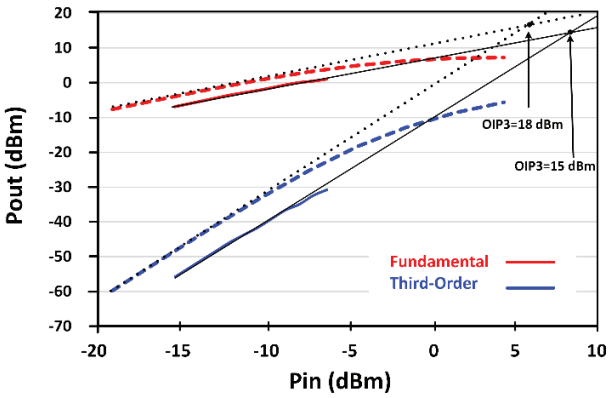


Fig. 15. Measured fundamental and $IM_3$ tone output power versus input power of the proposed mixer at LO frequency of 140 GHz and IF frequency of 2 GHz with 100-MHz tones space. Simulation results (dashed line) are also included.

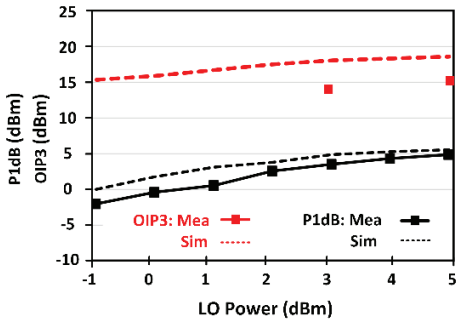


Fig. 16. Measured and simulated $OP_{1\,dB}$ and simulated $OIP_3$ versus LO power at LO frequency of 140 GHz and IF frequency of 2 GHz.

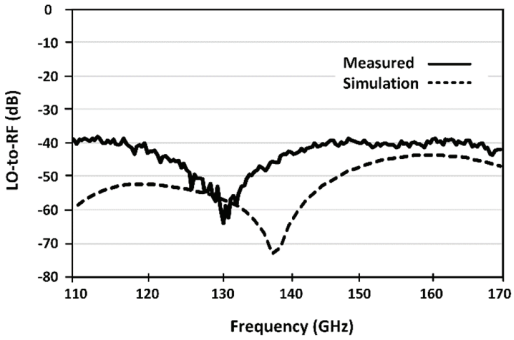


Fig. 17. Measured and simulated LO-to-RF port-to-port isolation.

simulation in a two-tone test procedure at an LO frequency of 140 GHz, and the two IF tones at 2 GHz are spaced by 100 MHz. From this figure, an 8-dBm $IIP_3$ and a 15-dBm $OIP_3$ can be observed.

The dependence of the 1-dB compression point and $OIP_3$ of the upconverter on the LO power is also examined. Fig. 16 plots the measured/simulated $OP_{1\,dB}$ and simulated $OIP_3$ of the mixer with LO power from −1 to 5 dBm. The $OP_{1\,dB}$ and $OIP_3$ are improved with higher LO power before the saturation of the mixer. This demonstrates that the linearity of the upconverters relies on the level of LO power as expected.

Fig. 17 displays the measured isolation between the mixer's LO input and RF output ports, along with the simulation

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TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH THE PRIOR-ART UPCONVERTERS

| | Topology | Technology ($f_t/f_{max}$) | Frequency (GHz) | Max. CG (dB) | Psat (dBm) | $P_{1dB}$ (dBm) | LO-RF Isolation (dB) | $P_{DC}$ (mW) | Chip Area ($mm^2$) | FOM |
|---|---|---|---|---|---|---|---|---|---|---|
| **[7] SSCL2024** | Gilbert Cell Up conv. | 55-nm SiGe (320/370) | 112-150 | 15 | 6.3 | 4.5 | - | 70-140 | 1.07 | -11.72 |
| **[8] MWCL17** | Gilbert Up conv. | 40-nm CMOS (195/254) | 105-135 | -4 | -9 | -11.5 | 35 | 9† | 0.63 | -17.29 |
| **[9] MTT15** | Gilbert I/Q Up conv. | 250nm InP HBT (350/650) | 115-155 | 6 | 2.5 | -2 | 27 | 78 | 0.25* | -16.92 |
| **[10] IJMWT18** | Gilbert I/Q Up conv. | 130-nm SiGe (230/280) | 119-152 | 9.8 | -1 | -4 | 31 | 53 | 0.22* | -14.34 |
| **[11] MTT17** | Gilbert Cell I/Q Up conv | 130-nm SiGe HBT (350/450) | 170-210 | -10 | -6 | -10 | - | 32 | 0.7 | -25.05 |
| **[12] SSCL2024** | Single-ended Passive Up conv. | 65-nm CMOS (200/250) | 110-160 | -11.5 | -11 | -12.5 | 20.4 | - | 0.35 | - |
| **[19] ESSCIRC19** | Gilbert Cell I/Q Up conv. PA | 130-nm SiGe (350/450) | 140-220 | 10 | 6.5 | -1 | - | 302 | 1.4 | -20.3 |
| **[20] RFIC18** | I/Q Up conv. 2 stg. PA | 40-nm CMOS (195/254) | 110-125 | 13.5 | - | 4.5 | - | 271 | 1.51 | -15.33 |
| **[21] RFIC19** | Gilbert Cell I/Q Up conv. 4 stg. PA | 22-nm FDSOI (347/371) | 132-139 | 18 | 2.8 | - | 24.7 | 196 | 1.44 | - |
| **[22] JCN21** | Gilbert Cell I/Q Up conv. 6 stg. PA | 130-nm SiGe (230/280) | 115-145 | 23 | 0 | -2 | - | 240 | 1.54 | -13.3 |
| **This Work** | **Cascode Up conv.** | **130-nm SiGe (250/390)** | **126-152** | **9.8** | **5.9** | **4.9** | **38** | **32†-69‡** | **0.22/0.07*** | **-11.04** |

* Core area † at small signal ‡ at Pout, max

results. The cascode setup of $T_1/T_2$ and $T_3/T_4$, with the balanced design (connecting the collectors of $T_3$ and $T_4$), in conjunction with a symmetric layout, improves isolation between the LO and RF ports in the mixer. The measured LO-to-RF isolation is larger than 38 dB over the full band.

The LO leakage to the input IF ports, $V_{IF+}$ and $V_{IF-}$, is negligible because the LO signal is blocked by the low-pass filter at IF port. The reflection coefficients of LO and RF ports were evaluated utilizing a PNA-X 67-GHz N5247A with WR6.5 VNA extenders. As depicted in Fig. 18, reasonable matching is attained at all three ports. The simulation and measurement results of the mixer's total current driven from a 3-V dc voltage supply for different LO power are shown in Fig. 19 at 140- and 2-GHz LO and IF frequency, respectively. It can be seen the current rises with increasing input IF power. At $P_{sat}$, the current varies in the range of 15–23 mA across various LO power levels. For the 3-V dc voltage, the mixer's maximum power consumption for 5-dBm LO power is 69 mW.

Table II provides a comparison of the performance of the up conversion mixers presented in this work with other published findings within a comparable frequency range.

Bilato et al. [7], Lee et al. [8], Carpenter et al. [9], [10], and Fritsche et al. [11] relate to up conversion mixers, while Stärke et al. [19], Lee et al. [20], Farid et al. [21], and Carpenter et al. [22] involve mixers followed by power amplifiers. Almost all the mixers listed in the table use the Gilbert architecture.

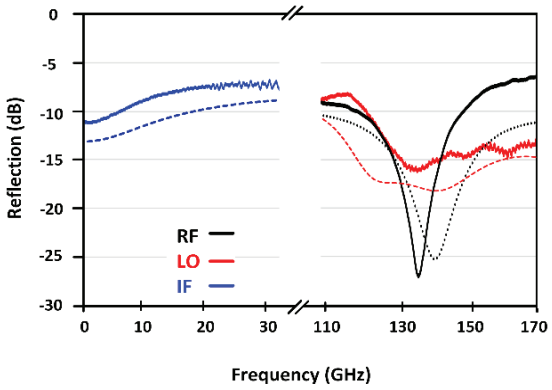


Fig. 18. Measured reflection of IF, LO, and RF ports. Simulation results (dashed line) are also included.

The main highlights of the present work are that it achieves the best linearity ($P_{1\,dB}$), high saturation power, and high LO-to-RF port isolation. The realized mixer has the smallest active chip area when compared to other state-of-the-art

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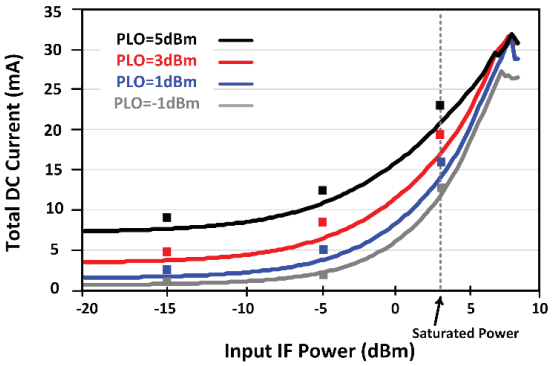


Fig. 19. Simulated (solid) and measured (squares) dc currents of the mixer versus input IF power at 140-GHz LO and 2-GHz IF frequency.

circuits, as shown in Table II. It also exhibits lower power consumption. Although the mixer in [8] and [11] consumes 9 and 32 mW of dc power, $P_{1\,\mathrm{dB}}$ and $P_{\mathrm{sat}}$ of this design are at least 10 dB larger than those in [8] and [11]. Bilato et al. [7] were implemented utilizing 55-nm SiGe technology and boasted a higher $f_t/f_{\max}$ compared to the present design (130-nm SiGe), exhibiting greater gain owing to the pre-IF amplifier. It requires a much larger chip area (almost tenfold) and more power (nearly doubled) than our design. Compared to the passive single-ended mixer with controlled LO feedthrough presented in [12], which demonstrated a flat LO leakage profile over a similar frequency range, the proposed design achieves a significant enhancement in output power and linearity, while maintaining a balanced architecture that inherently improves LO-RF isolation.

In [19], [20], [21], and [22], the mixer with stages of power amplifier offers higher gain and saturation power as expected. However, this comes at the expense of increased dc power consumption and larger chip size.

The figures of merit (FOMs) [23], [24] have been assessed to ensure an equitable comparison between the presented mixer and others. The FOM considers CG, linearity ($P_{1\,\mathrm{dB}}$), and dc power usage ($P_{\mathrm{dc}}$) as the key factors dominating the performance of up conversion mixers

$$\mathrm{FOM\,(dB)} = 10\log\frac{10^{\frac{\mathrm{CG}}{20}}.10^{\frac{P_{1\,\mathrm{dB}}}{20}}}{\frac{P_{\mathrm{dc}}}{1\ \mathrm{mW}}}. \tag{6}$$

The presented mixer has demonstrated the best performance in FOM, attributed to its low dc power dissipation and high linearity compared to all previously documented works listed in Table II.

## IV. Conclusion

This article introduces a D-band balanced cascode up conversion mixer, fabricated using a 130-nm SiGe HBT process, which showcases significant improvements in key performance metrics, such as output power, linearity, and chip size. The cascode configuration employs a double mixing technique, where the LO and IF signals are remixed, leading to enhanced overall performance. This design is particularly well-suited for high-speed wireless communication systems, offering a compact footprint and low power consumption, which are critical for integration into modern communication platforms.

Additionally, a phase quadrature version of the mixer has been successfully integrated into a transmitter system, demonstrating its seamless compatibility with other components and further underscoring its practical utility.

## Acknowledgment

The authors would like to thank Infineon Technologies AG for the fabrication of the chips, and the support from Klaus Aufinger, Franz Dielacher, and Siegfried Krainer is highly appreciated. This work is partly supported by the European Union under the project 101096302 – 6GTandem, and partly supported by the Vinnova center WiTECH, project HiComin.

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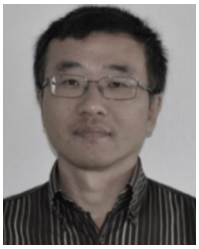

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